

3.3 V FULL-DUPLEX RS-485 DRIVERS AND RECEIVERS

FEATURES

- **1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)**
- **Bus-Pin ESD Protection Exceeds 15 kV HBM**
- **Optional Driver Output Transition Times for Signaling Rates⁽¹⁾ of 1 Mbps, 5 Mbps and 26 Mbps**
- **Low-Current Standby Mode: < 1 μ A**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **5-V Tolerant Inputs**
- **Bus Idle, Open, and Short Circuit Failsafe**
- **Driver Current Limiting and Thermal Shutdown**
- **Designed for RS-422 and RS-485 Networks**
- **5-V Devices available, SN65HVD50-59**

(1) Line Signaling Rate is the number of voltage transitions made per second expressed in units of bps (bits per second).

APPLICATIONS

- **Utility Meters**
- **DTE/DCE Interfaces**
- **Industrial, Process, and Building Automation**
- **Point-of-Sale (POS) Terminals and Networks**

DESCRIPTION

The SN65HVD3X devices are 3-state differential line drivers and differential-input line receivers that operate with 3.3-V power supply.

IMPROVED REPLACEMENT FOR:

Part Number	Replace with	
xxx3491 xxx3490	SN65HVD33: SN65HVD30:	Better ESD protection (15kV vs 2kV or not specified) Higher Signaling Rate (26Mbps vs 20Mbps) Fractional Unit Load (64 Nodes vs 32)
MAX3491E MAX3490E	SN65HVD33: SN65HVD30:	Higher Signaling Rate (26Mbps vs 12Mbps) Fractional Unit Load (64 Nodes vs 32)
MAX3076E MAX3077E	SN65HVD33: SN65HVD30:	Higher Signaling Rate (26Mbps vs 16Mbps) Lower Standby Current (1 μ A vs 10 μ A)
MAX3073E MAX3074E	SN65HVD34: SN65HVD31:	Higher Signaling Rate (5Mbps vs 500kbps) Lower Standby Current (1 μ A vs 10 μ A)
MAX3070E MAX3071E	SN65HVD35: SN65HVD32:	Higher Signaling Rate (1Mbps vs 250kbps) Lower Standby Current (1 μ A vs 10 μ A)

Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and inter-operation with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11 and ISO 8482:1993 standard-compliant devices.

The SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36 and SN65HVD37 are fully enabled with no external enabling pins.

The SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38, and SN65HVD39 have active-high driver enables and active-low receiver enables. A low, less than 1 μ A, standby current can be achieved by disabling both the driver and receiver.

All devices are characterized for ambient temperatures from -40°C to 85°C . Low power dissipation allows operation at temperatures up to 105°C or 125°C , depending on package option.

The preview devices SN65HVD36 and SN65HVD38 implement receiver equalization technology for improved jitter performance on differential bus applications with data rates up to 20 Mbps at cable lengths up to 160 meters.

The preview devices SN65HVD37 and SN65HVD39 implement receiver equalization technology for improved jitter performance on differential bus applications with data rates in the range of 1 to 5 Mbps at cable lengths up to 1000 meters.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN65HVD30 – SN65HVD39

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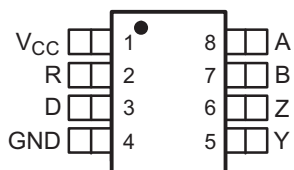


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

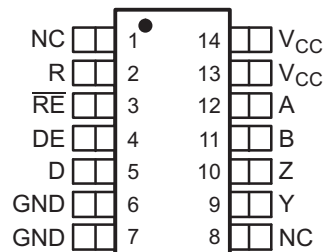
SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36, SN65HVD37

D PACKAGE (TOP VIEW)

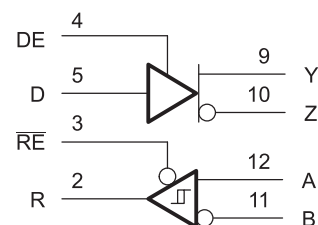


SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38, SN65HVD39

D PACKAGE (TOP VIEW)

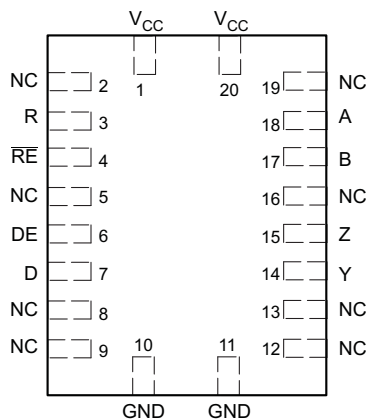


NC - No internal connection

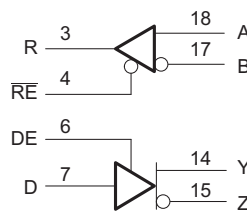


SN65HVD33

RHL PACKAGE (TOP VIEW)



NC - No internal connection



AVAILABLE OPTIONS

SIGNALING RATE	UNIT LOADS	RECEIVER EQUALIZATION	ENABLES	BASE PART NUMBER	SOIC MARKING
26 Mbps		No	No	SN65HVD30	VP30
5 Mbps	1/8	No	No	SN65HVD31	VP31
1 Mbps	1/8	No	No	SN65HVD32	VP32
26 Mbps		No	Yes	SN65HVD33	65HVD33
5 Mbps	1/8	No	Yes	SN65HVD34	65HVD34
1 Mbps	1/8	No	Yes	SN65HVD35	65HVD35
26 Mbps		Yes	No	SN65HVD36	PREVIEW
5 Mbps	1/8	Yes	No	SN65HVD37	PREVIEW
26 Mbps		Yes	Yes	SN65HVD38	PREVIEW
5 Mbps	1/8	Yes	Yes	SN65HVD39	PREVIEW

ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range unless otherwise noted^{(1) (2)}

		UNIT
V_{CC}	Supply voltage range	-0.3 V to 6 V
$V_{(A)}, V_{(B)}, V_{(Y)}, V_{(Z)}$	Voltage range at any bus terminal (A, B, Y, Z)	-9 V to 14 V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 Ω . See Figure 12 (A, B, Y, Z) ⁽³⁾	-50 to 50 V
V_I	Input voltage range (D, DE, \overline{RE})	-0.5 V to 7 V
$P_{D(cont)}$	Continuous total power dissipation	Internally limited ⁽⁴⁾
I_O	Output current (receiver output only, R)	11 mA

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) This tests survivability only and the output state of the receiver is not specified.
- (4) The thermal shutdown protection circuit internally limits the continuous total power dissipation. Thermal shutdown typically occurs when the junction temperature reaches 165°C.

DISSIPATION RATINGS

PACKAGE	JEDEC THERMAL MODEL	$T_A < 25^\circ\text{C}$ RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ RATING	$T_A = 105^\circ\text{C}$ RATING	$T_A = 125^\circ\text{C}$ RATING
SOIC (D) 8 pin	Low k	625 mW	5 mW/°C	325 mW		
	High k	1000 mW	8 mW/°C	520 mW	360 mW	
SOIC (D) 14 pin	Low k	765 mW	6.1 mW/°C	400 mW	275 mW	
	High k	1350 mW	10.8 mW/°C	705 mW	485 mW	270 mW
QFN (RHL) 20 pin	High k	1710 mW	13.7 mW/°C	890 mW	6150 mW	340 mW

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)	$-7^{(1)}$		12	
$1/t_{UI}$	Signaling rate	SN65HVD30, SN65HVD33, SN65HVD36, SN65HVD38		26	Mbps
		SN65HVD31, SN65HVD34, SN65HVD37, SN65HVD39		5	
		SN65HVD32, SN65HVD35		1	
R_L	Differential load resistance	54	60		Ω
V_{IH}	High-level input voltage	D, DE, \overline{RE}		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, \overline{RE}		0.8	
V_{ID}	Differential input voltage	-12		12	
I_{OH}	High-level output current	Driver		-60	mA
		Receiver		-8	
I_{OL}	Low-level output current	Driver		60	mA
		Receiver		8	
T_J	Junction temperature	-40		150	$^{\circ}\text{C}$

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
Human body model	Bus terminals and GND		± 16		kV
Human body model ⁽²⁾	All pins		± 4		
Charged-device-model ⁽³⁾	All pins		± 1		

(1) All typical values at 25°C with 3.3-V supply.

(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT	
$V_{I(K)}$	Input clamp voltage	$I_I = -18$ mA		-1.5			V	
$ V_{OD(SS)} $	Steady-state differential output voltage	$I_O = 0$		2.5		V_{CC}	V	
		$R_L = 54$ Ω , See Figure 1 (RS-485)		1.5	2			
		$R_L = 100$ Ω , See Figure 1 , ⁽²⁾ (RS-422)		2	2.3			
		$V_{test} = -7$ V to 12 V, See Figure 2		1.5				
$\Delta V_{OD(SS)} $	Change in magnitude of steady-state differential output voltage between states	$R_L = 54$ Ω , See Figure 1 and Figure 2		-0.2		0.2	V	
$V_{OD(RING)}$	Differential Output Voltage overshoot and undershoot	$R_L = 54$ Ω , $C_L = 50$ pF, See Figure 5 and Figure 3				10% ⁽³⁾	V	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD30, HVD33, HVD36, HVD38	See Figure 4	0.5			V	
		HVD31, HVD34, HVD37, HVD39, HVD32, HVD35		0.25				
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 4		1.6		2.3	V	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-0.05		0.05		
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current	HVD30, HVD31, HVD32, HVD36, HVD37		$V_{CC} = 0$ V, V_Z or $V_Y = 12$ V, Other input at 0 V		90	μ A	
				$V_{CC} = 0$ V, V_Z or $V_Y = -7$ V, Other input at 0 V		-10		
		HVD33, HVD34, HVD35, HVD38, HVD39		Other input at 0 V	$V_{CC} = 3$ V or 0 V, DE = 0 V, V_Z or $V_Y = 12$ V			90
					$V_{CC} = 3$ V or 0 V, DE = 0 V, V_Z or $V_Y = -7$ V			-10
$I_{Z(S)}$ or $I_{Y(S)}$	Short Circuit output current ⁽⁴⁾			Other input at 0 V	V_Z or $V_Y = -7$ V	-250	250	mA
					V_Z or $V_Y = 12$ V	-250	250	
I_I	Input current	D, DE		0		100	μ A	
$C_{(OD)}$	Differential output capacitance	$V_{OD} = 0.4 \sin(4E6\pi t) + 0.5$ V, DE at 0 V				16	pF	

(1) All typical values are at 25°C and with a 3.3-V supply.

 (2) V_{CC} is 3.3 Vdc \pm 5%

(3) 10% of the peak-to-peak differential output voltage swing, per TIA/EIA-485

(4) Under some conditions of short-circuit to negative voltages, output currents exceeding the ANSI TIA/EIA-485-A maximum current of 250 mA may occur. Continuous exposure may affect device reliability.

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DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	HVD30, HVD33, HVD36, HVD38	4	10	18	ns
		HVD31, HVD34, HVD37, HVD39	25	38	65	
		HVD32, HVD35	120	175	305	
t _{PHL}	Propagation delay time, high-to-low-level output	HVD30, HVD33, HVD36, HVD38	4	9	18	ns
		HVD31, HVD34, HVD37, HVD39	25	38	65	
		HVD32, HVD35	120	175	305	
t _r	Differential output signal rise time	HVD30, HVD33, HVD36, HVD38	2.5	5	12	ns
		HVD31, HVD34, HVD37, HVD39	20	37	60	
		HVD32, HVD35	120	185	300	
t _f	Differential output signal fall time	HVD30, HVD33, HVD36, HVD38	2.5	5	12	ns
		HVD31, HVD34, HVD37, HVD39	20	35	60	
		HVD32, HVD35	120	180	300	
t _{sk(p)}	Pulse skew ((t _{PHL} – t _{PLH}))	HVD30, HVD33, HVD36, HVD38		0.6		ns
		HVD31, HVD34, HVD37, HVD39		2.0		
		HVD32, HVD35		5.1		
t _{PZH1}	Propagation delay time, high-impedance-to-high-level output	HVD33, HVD38			45	ns
		HVD34, HVD39			235	
		HVD35			490	
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD33, HVD38			25	ns
		HVD34, HVD39			65	
		HVD35			165	
t _{PZL1}	Propagation delay time, high-impedance-to-low-level output	HVD33, HVD38			35	ns
		HVD34, HVD39			190	
		HVD35			490	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD33, HVD38			30	ns
		HVD34, HVD39			120	
		HVD35			290	
t _{PZH2}	Propagation delay time, standby-to-high-level output	R _L = 110 Ω, \overline{RE} at 3 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z See Figure 6			4000	ns
t _{PZL2}	Propagation delay time, standby-to-low-level output	R _L = 110 Ω, \overline{RE} at 3 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y See Figure 7			4000	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{IT+}	Positive-going differential input threshold voltage	$I_O = -8$ mA			-0.02	V	
V_{IT-}	Negative-going differential input threshold voltage	$I_O = 8$ mA	-0.20			V	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV	
V_{IK}	Enable-input clamp voltage	$I_I = -18$ mA	-1.5			V	
V_O	Output voltage	$V_{ID} = 200$ mV, $I_O = -8$ mA, See Figure 8	2.4			V	
		$V_{ID} = -200$ mV, $I_O = 8$ mA, See Figure 8			0.4	V	
$I_{O(Z)}$	High-impedance-state output current	$V_O = 0$ or V_{CC} , \overline{RE} at V_{CC}	-1		1	μ A	
I_A or I_B	Bus input current	HVD31, HVD32, HVD34, HVD35, HVD37, HVD39	Other input at 0V	V_A or $V_B = 12$ V	0.05	0.1	mA
				V_A or $V_B = 12$ V, $V_{CC} = 0$ V	0.06	0.1	
				V_A or $V_B = -7$ V	-0.10	-0.04	
				V_A or $V_B = -7$ V, $V_{CC} = 0$ V	-0.10	-0.03	
	HVD30, HVD33, HVD36, HVD38	Other input at 0V	V_A or $V_B = 12$ V	0.20	0.35	mA	
			V_A or $V_B = 12$ V, $V_{CC} = 0$ V	0.24	0.4		
			V_A or $V_B = -7$ V	-0.35	-0.18		
			V_A or $V_B = -7$ V, $V_{CC} = 0$ V	-0.25	-0.13		
I_{IH}	Input current, \overline{RE}	$V_{IH} = 0.8$ V or 2 V	-60			μ A	
C_{ID}	Differential input capacitance	$V_{ID} = 0.4 \sin(4E6\pi t) + 0.5$ V, DE at 0 V		15		pF	

(1) All typical values are at 25°C and with a 3.3-V supply.

SUPPLY CURRENT CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT		
I_{CC}	Supply current	D at 0 V or V_{CC} and No Load			2.1	mA		
					HVD30			
					HVD31, HVD32			
		HVD36, HVD37				7.9	mA	
		HVD33						
		HVD34, HVD35						
		HVD38, HVD39	\overline{RE} at 0 V, D at 0 V or V_{CC} , DE at 0 V, No load (Receiver enabled and driver disabled)				3.8	mA
		HVD33, HVD34, HVD35, HVD38, HVD39	\overline{RE} at V_{CC} , D at V_{CC} , DE at 0 V, No load (Receiver disabled and driver disabled)	0.022		1	μ A	
		HVD33				2.1	mA	
		HVD34, HVD35	\overline{RE} at 0 V, D at 0 V or V_{CC} , DE at V_{CC} , No load (Receiver enabled and driver enabled)			6.5		
		HVD38				3.5		
		HVD39				8		
		HVD33				1.8		
		HVD34, HVD35	\overline{RE} at V_{CC} , D at 0 V or V_{CC} , DE at V_{CC} , No load (Receiver disabled and driver enabled)			6.2		
HVD38				2.5				
HVD39				7				

(1) All typical values are at 25°C and with a 3.3-V supply.

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RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	HVD30, HVD33, HVD36, HVD38		26	45	ns
		HVD31, HVD32, HVD34, HVD35, HVD37, HVD39		47	70	
t _{PHL}	Propagation delay time, high-to-low-level output	HVD30, HVD33, HVD36, HVD38	V _{ID} = -1.5 V to 1.5 V, C _L = 15 pF, See Figure 9	29	45	
		HVD31, HVD32, HVD34, HVD35, HVD37, HVD39		49	70	
t _{sk(p)}	Pulse skew (t _{PHL} – t _{PLH})	HVD30, HVD33, HVD36, HVD37, HVD38, HVD39		7		
		HVD31, HVD34, HVD32, HVD35		10		
t _r	Output signal rise time			5		
t _f	Output signal fall time			6		
t _{PHZ}	Output disable time from high level	DE at 3 V		C _L = 15 pF, See Figure 10	20	
t _{PZH1}	Output enable time to high level	DE at 0 V			20	
t _{PZH2}	Propagation delay time, standby-to-high-level output	DE at 0 V			4000	
t _{PLZ}	Output disable time from low level	DE at 3 V		C _L = 15 pF, See Figure 11	20	
t _{PZL1}	Output enable time to low level	DE at 0 V			20	
t _{PZL2}	Propagation delay time, standby-to-low-level output	DE at 0 V			4000	

(1) All typical values are at 25°C and with a 3.3-V supply

RECEIVER EQUALIZATION CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	DEVICE	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{j(pp)}	Peak-to-peak eye-pattern jitter Pseudo-random NRZ code with a bit pattern length of 2 ¹⁶ –1, Belden 3105A cable	25 Mbps	0 m	HVD36, HVD38		PREVIEW
			100 m	HVD33 ⁽²⁾		PREVIEW
				HVD36, HVD38		PREVIEW
			150 m	HVD33 ⁽²⁾		PREVIEW
				HVD36, HVD38		PREVIEW
			200 m	HVD33 ⁽²⁾		PREVIEW
				HVD36, HVD38		PREVIEW
			10 Mbps	200 m	HVD33 ⁽²⁾	
		HVD36, HVD38			PREVIEW	
		250 m		HVD33 ⁽²⁾		PREVIEW
				HVD36, HVD38		PREVIEW
		300 m		HVD33 ⁽²⁾		PREVIEW
				HVD36, HVD38		PREVIEW
		5 Mbps	500 m	HVD34 ⁽²⁾		PREVIEW
				HVD37, HVD39		PREVIEW
		3 Mbps	500 m	HVD33 ⁽²⁾		PREVIEW
				HVD34 ⁽²⁾		PREVIEW
				HVD36, HVD38		PREVIEW
				HVD37, HVD39		PREVIEW
		1 Mbps	1000 m	HVD34 ⁽²⁾		PREVIEW
HVD37, HVD39				PREVIEW		

 (1) All typical values are at V_{CC} = 5 V, and temperature = 25°C.

(2) The HVD33 and the HVD34 do not have receiver equalization but are specified for comparison.

DEVICE POWER DISSIPATION – P_D

PARAMETER		TEST CONDITIONS	VALUE	UNITS		
θ _{JA}	Junction-to-Ambient Thermal Resistance	SOIC-8	JEDEC Low-K model	231	°C/W	
			JEDEC High-K model	135		
		SOIC-14	JEDEC Low-K model	163		
			JEDEC High-K model	92		
QFN-20		73				
θ _{JB}	Junction-to- Board Thermal Resistance	SOIC-8	44	°C/W		
		SOIC-14	61			
		QFN-20				
θ _{JC}	Junction-to-Case Thermal Resistance	SOIC-8	43	°C/W		
		SOIC-14	59			
		QFN-20	14			
P _D	Power Dissipation Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: HVD30,33 at 25 Mbps, HVD31,34 at 5 Mbps, HVD32,35 at 1 Mbps	Typical	HVD30,33	V _{CC} = 3.3V, T _J = 25°C, R _L = 60 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver)	mW	
			HVD31,34			
			HVD32,35			
		Worst-case	HVD30,33	V _{CC} = 3.6V, T _J = 140°C, R _L = 54 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver)	197	mW
			HVD31,34		213	
			HVD32,35		248	
T _{SD}	Thermal Shut-down Junction Temperature		170	°C		

PARAMETER MEASUREMENT INFORMATION

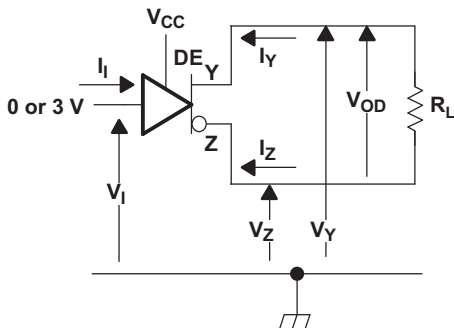


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

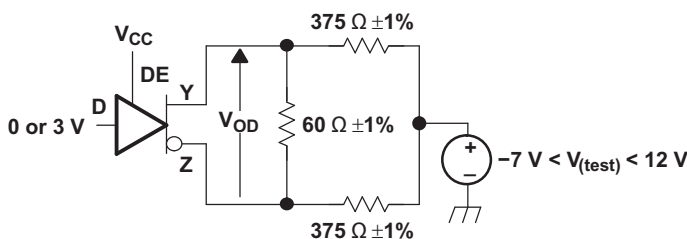


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

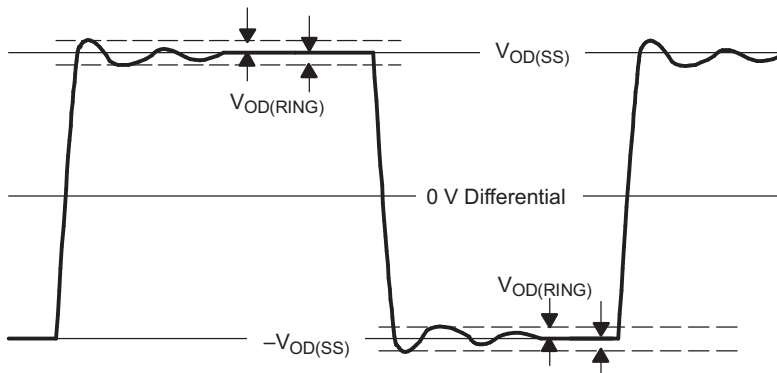
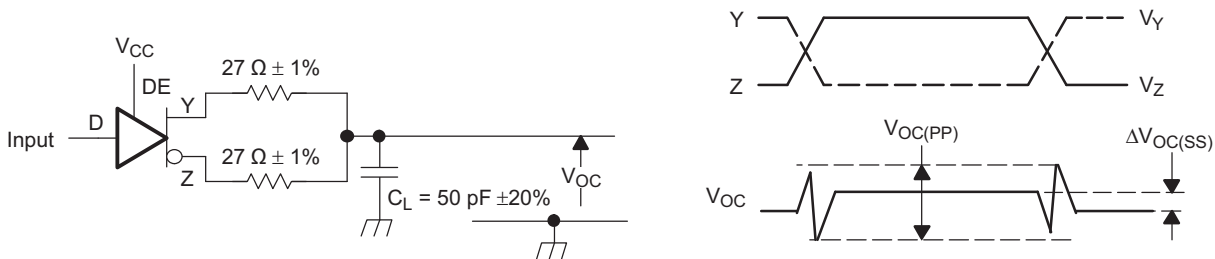


Figure 3. $V_{OD(RING)}$ Waveform and Definitions

$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

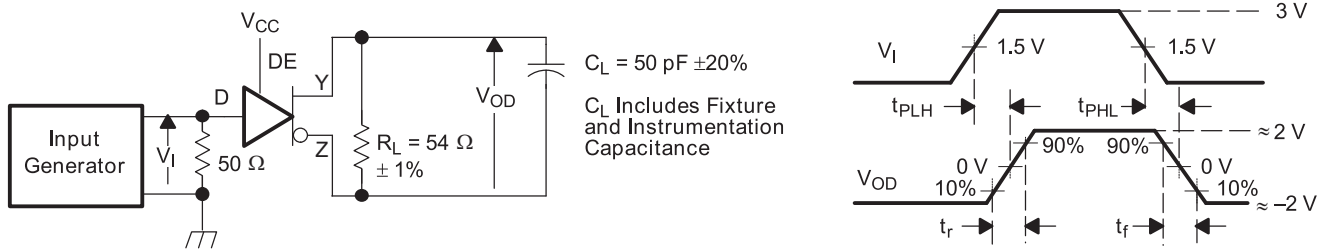


C_L Includes Fixture and Instrumentation Capacitance

Input: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6ns$, $t_f < 6ns$, $Z_O = 50 \Omega$

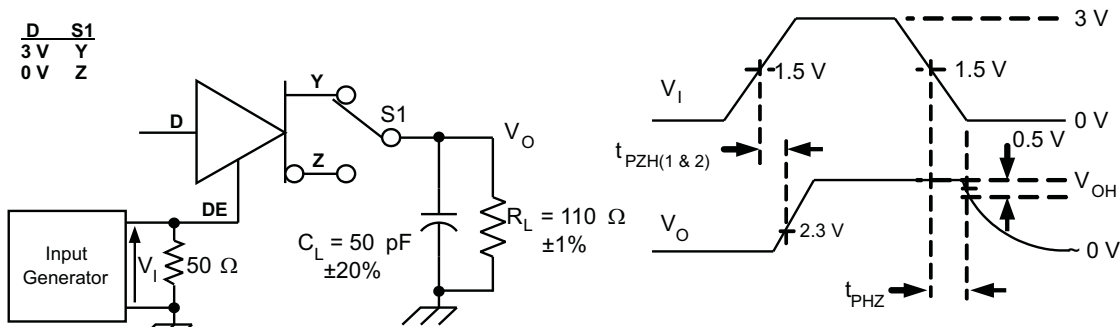
Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6 \text{ ns}$, $t_f < 6 \text{ ns}$, $Z_0 = 50 \Omega$

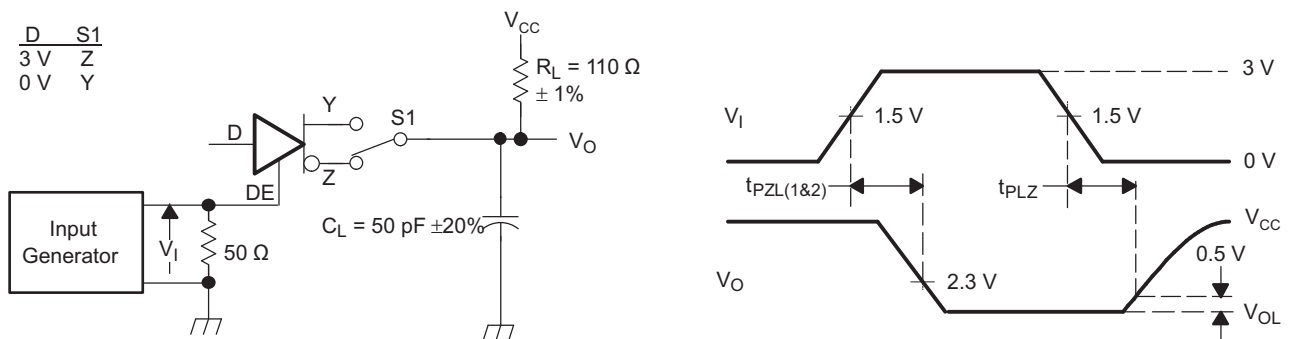
Figure 5. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 50 kHz, 50% Duty Cycle, $t_r < 6 \text{ ns}$, $t_f < 6 \text{ ns}$, $Z_0 = 50 \Omega$

C_L Includes Fixture and Instrumentation Capacitance

Figure 6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 50 kHz, 50% Duty Cycle, $t_r < 6 \text{ ns}$, $t_f < 6 \text{ ns}$, $Z_0 = 50 \Omega$

C_L Includes Fixture and Instrumentation Capacitance

Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

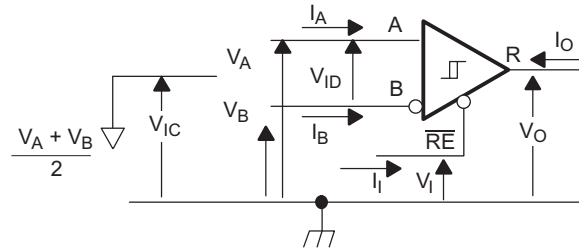


Figure 8. Receiver Voltage and Current Definitions

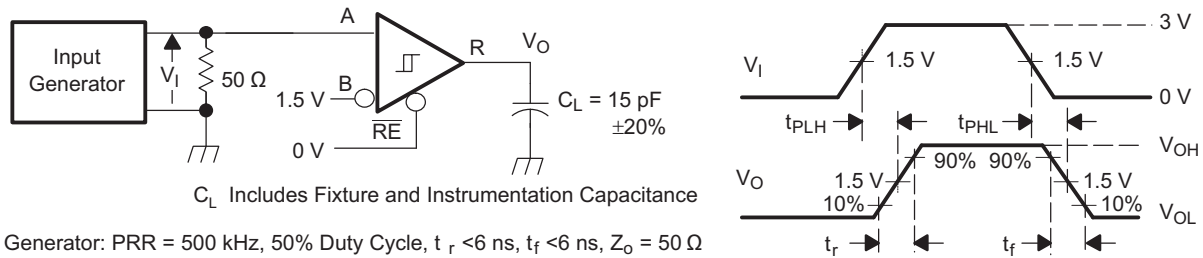


Figure 9. Receiver Switching Test Circuit and Voltage Waveforms

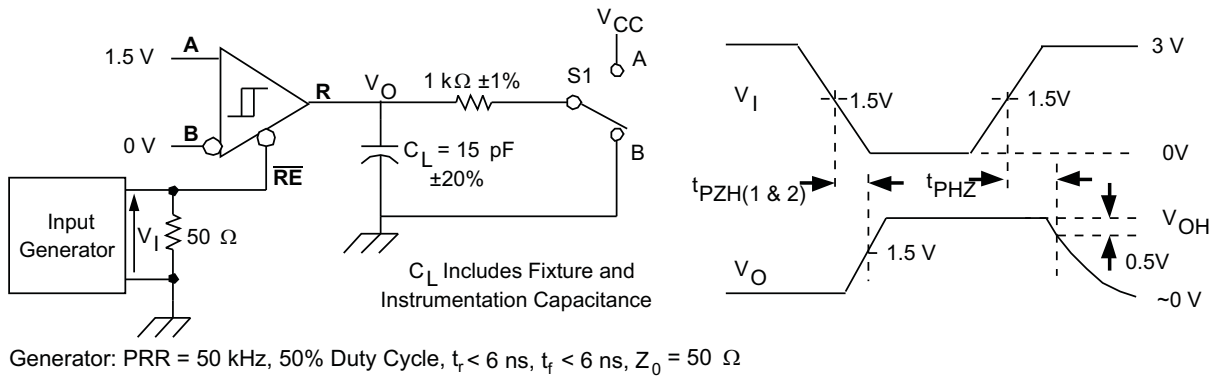


Figure 10. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

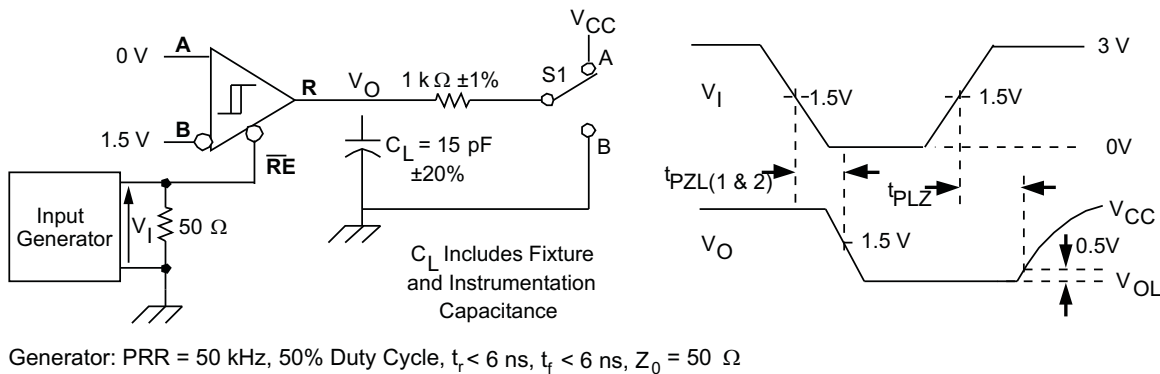


Figure 11. Receiver Enable Time From Standby (Driver Disabled)

PARAMETER MEASUREMENT INFORMATION (continued)

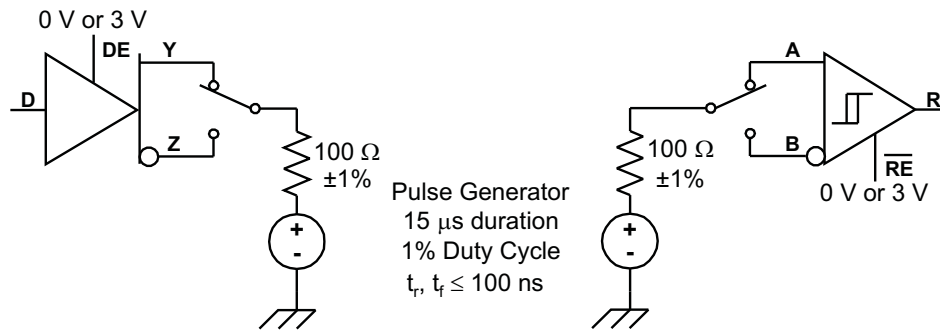


Figure 12. Test Circuit, Transient Over Voltage Test

DEVICE INFORMATION

LOW-POWER STANDBY MODE

When both the driver and receiver are disabled (\overline{DE} low and \overline{RE} high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

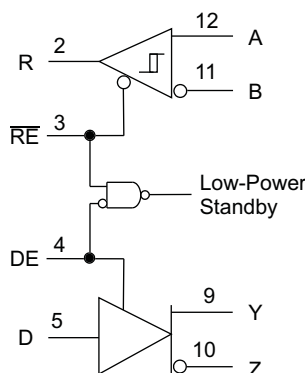


Figure 13. Low-Power Standby Logic Diagram

If only the driver is re-enabled (\overline{DE} transitions to high) the driver outputs are driven according to the D input after the enable times given by t_{PZH2} and t_{PZL2} in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs default to A high and B low, in accordance with the driver failsafe feature.

If only the receiver is re-enabled (\overline{RE} transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by t_{PZH2} and t_{PZL2} in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

FUNCTION TABLES
**SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38,
SN65HVD39 DRIVER**

INPUTS		OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

**SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38,
SN65HVD39 RECEIVER**

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE \overline{RE}	OUTPUT R
$V_{ID} \leq -0.2\text{ V}$	L	L
$-0.2\text{ V} < V_{ID} < -0.02\text{ V}$	L	?
$-0.02\text{ V} \leq V_{ID}$	L	H
X	H or open	Z
Open Circuit	L	H
Idle circuit	L	H
Short Circuit, $V_{(A)} = V_{(B)}$	L	H

**SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36,
SN65HVD37 DRIVER**

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H
Open	L	H

**SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36,
SN65HVD37 RECEIVER**

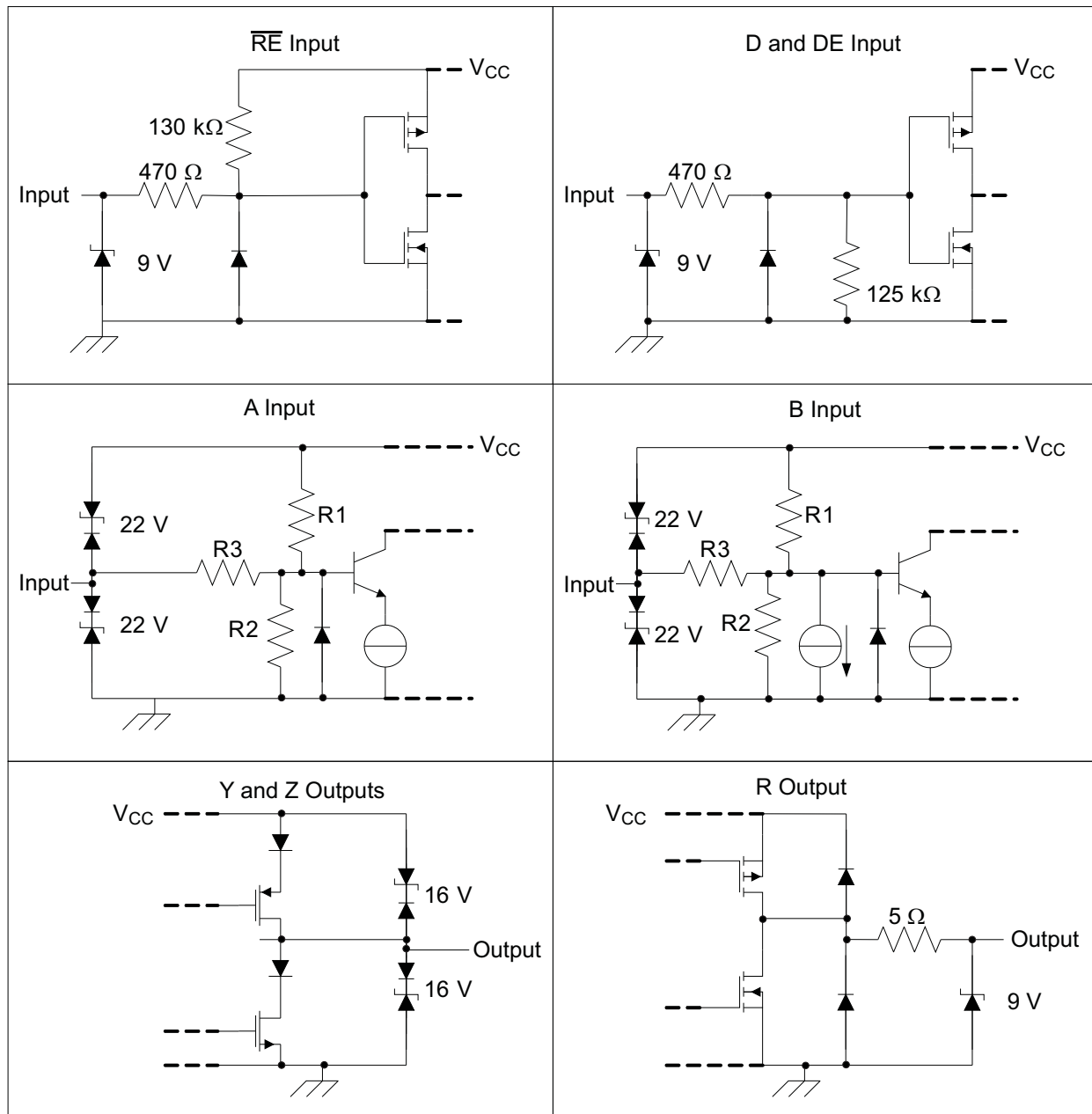
DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	OUTPUT R
$V_{ID} \leq -0.2\text{ V}$	L
$-0.2\text{ V} < V_{ID} < -0.02\text{ V}$?
$-0.02\text{ V} \leq V_{ID}$	H
Open Circuit	H
Idle circuit	H
Short Circuit, $V_{(A)} = V_{(B)}$	H

SN65HVD30 – SN65HVD39

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EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD30, SN65HVD33, SN65HVD36, SN65HVD38	9 kΩ	45 kΩ
SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35, SN65HVD37, SN65HVD38, SN65HVD39	36 kΩ	180 kΩ

TYPICAL CHARACTERISTICS

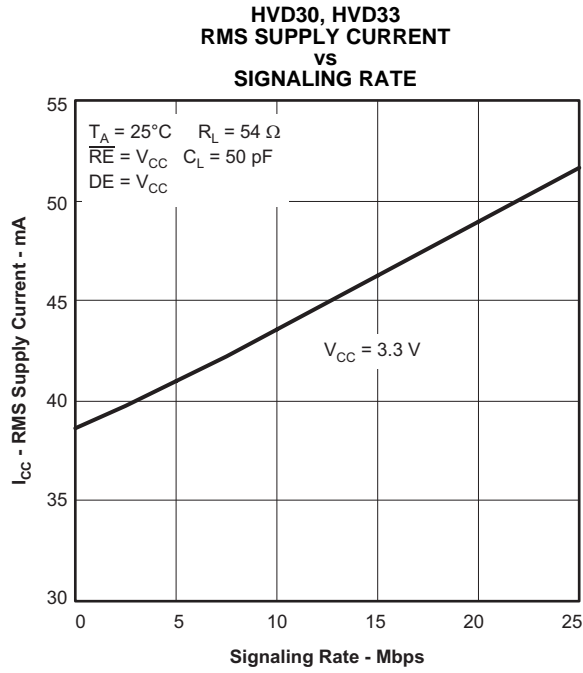


Figure 14.

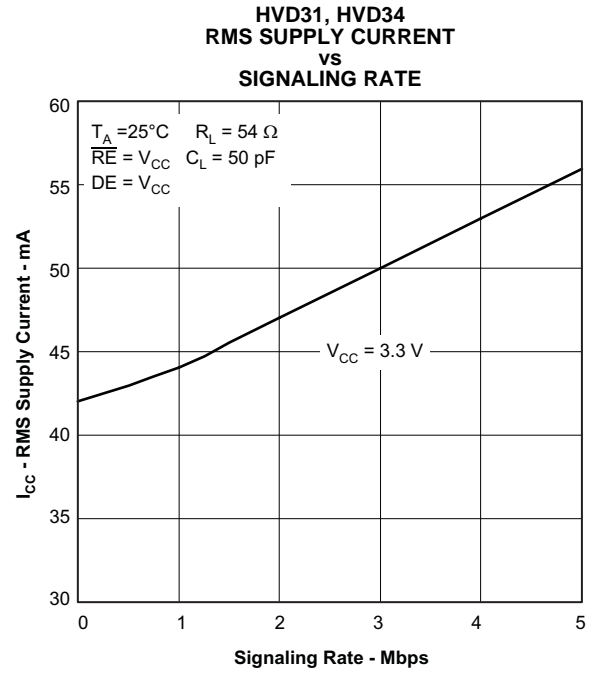


Figure 15.

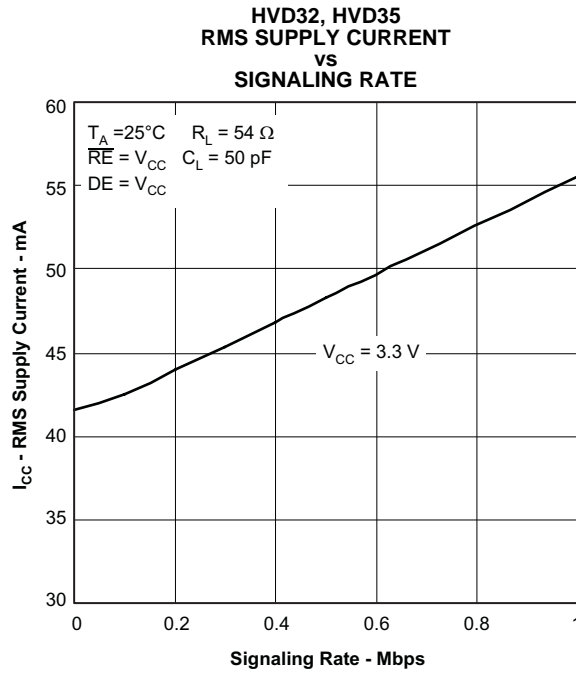
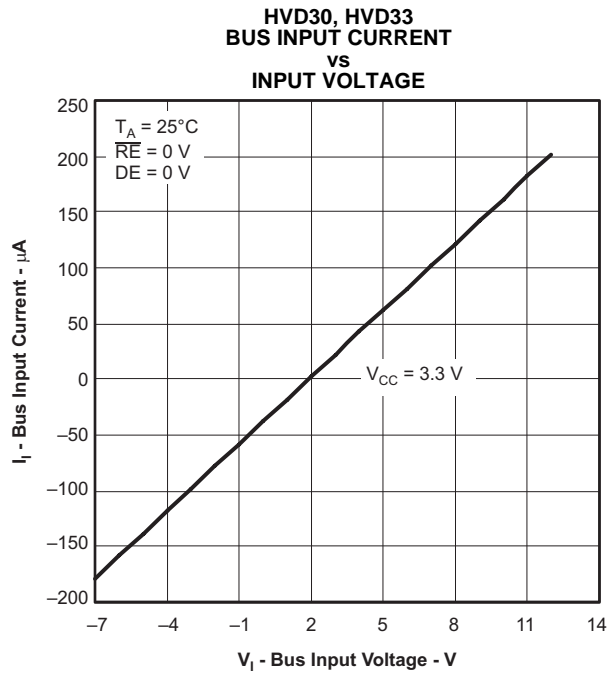
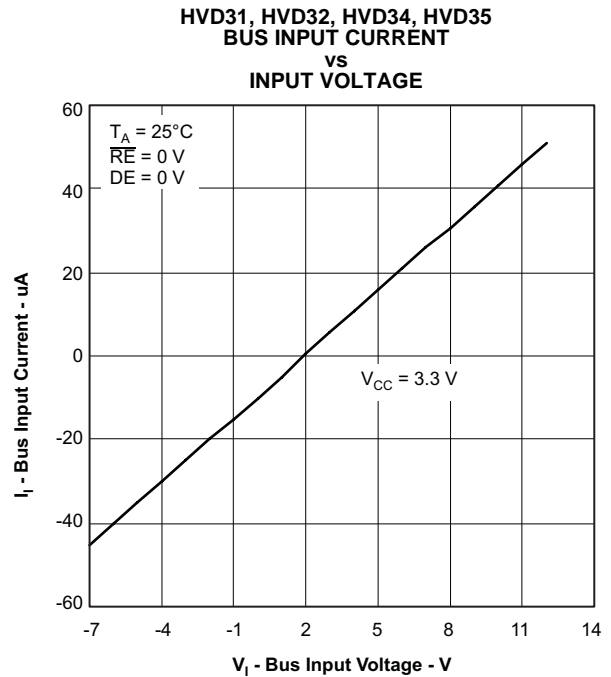
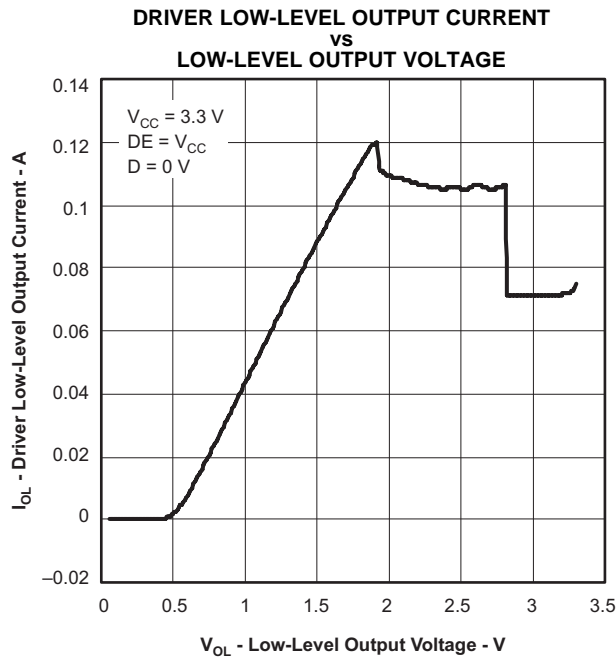
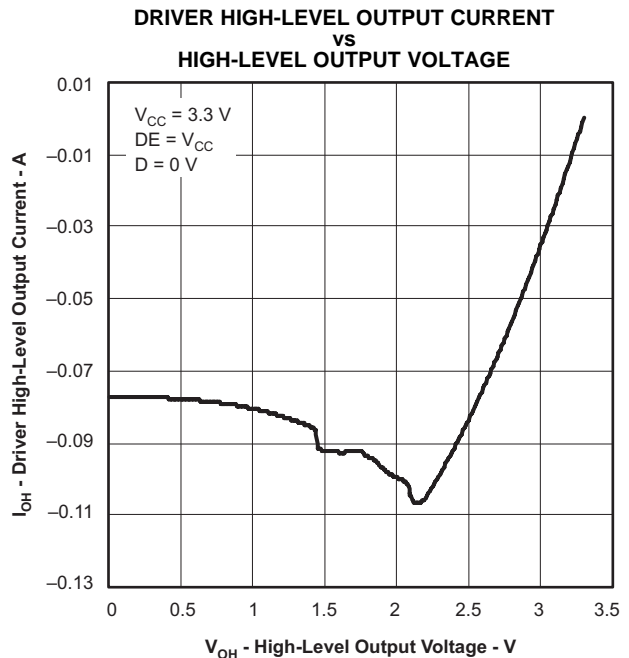


Figure 16.

TYPICAL CHARACTERISTICS (continued)

Figure 17.

Figure 18.

Figure 19.

Figure 20.

TYPICAL CHARACTERISTICS (continued)

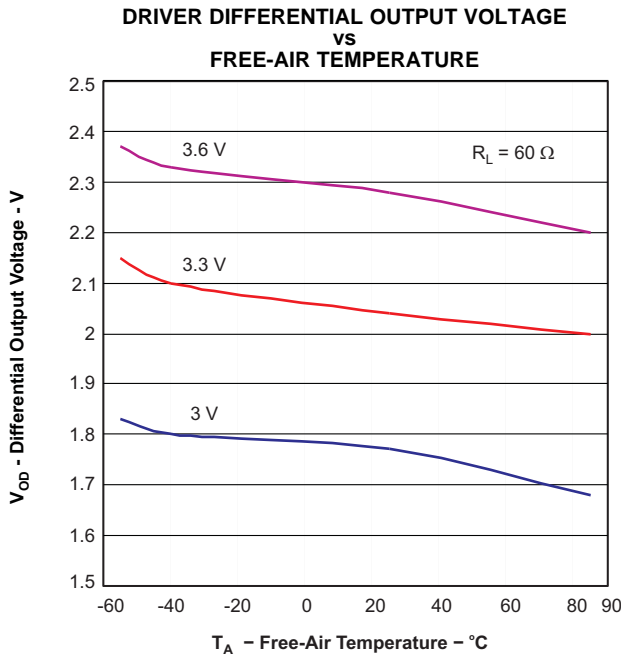


Figure 21.

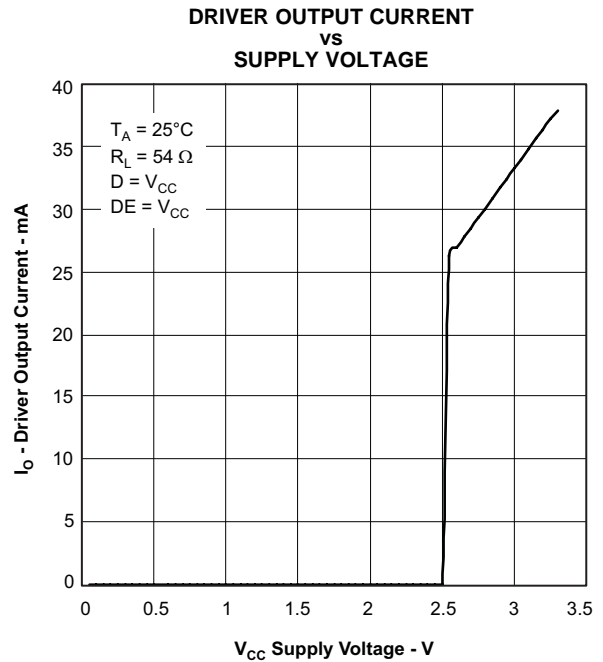


Figure 22.

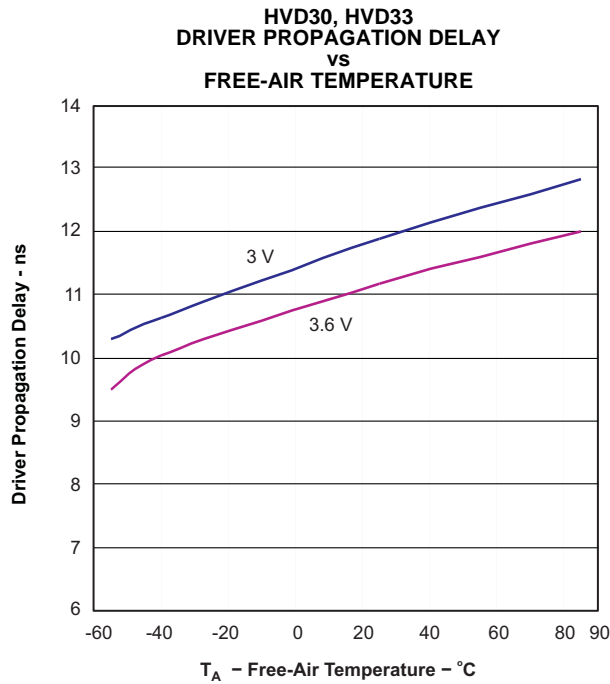


Figure 23.

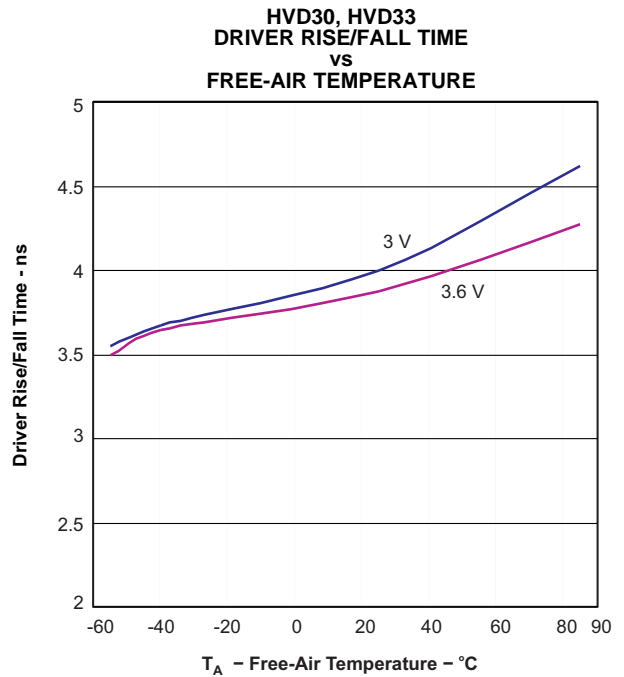
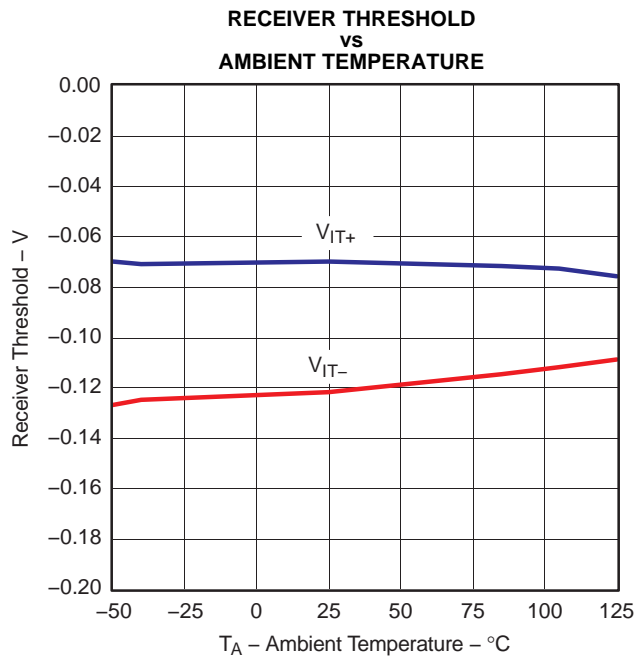
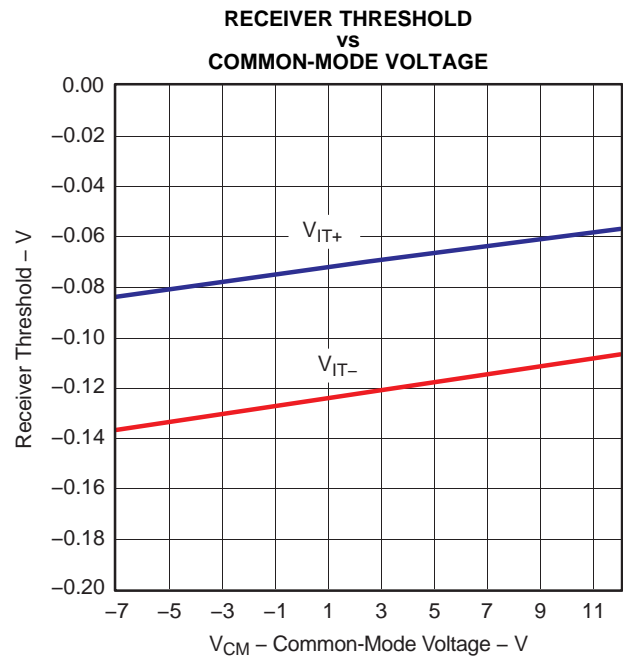
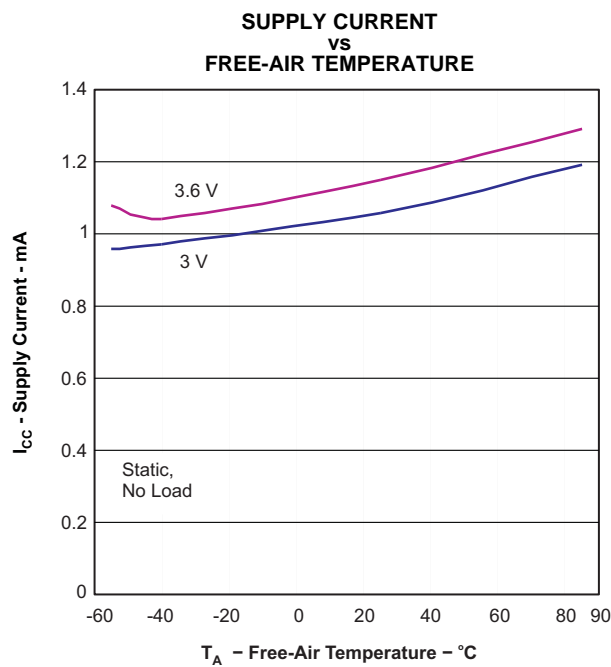
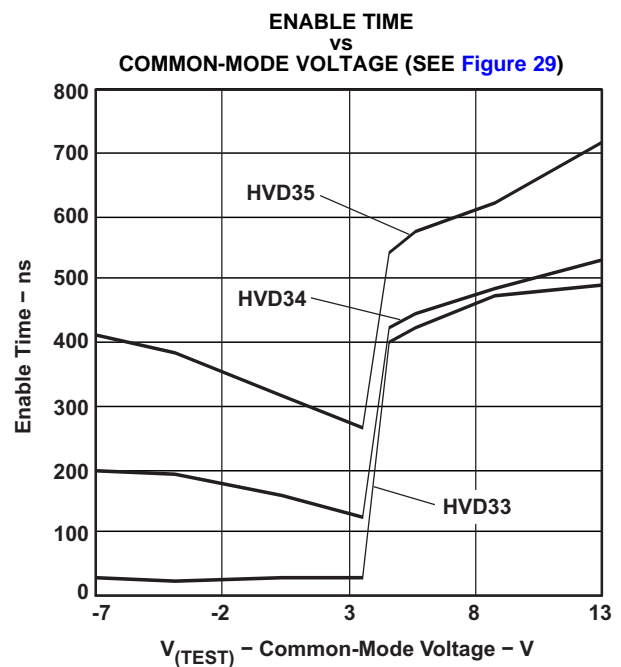


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Figure 25.

Figure 26.

Figure 27.

Figure 28.

TYPICAL CHARACTERISTICS (continued)

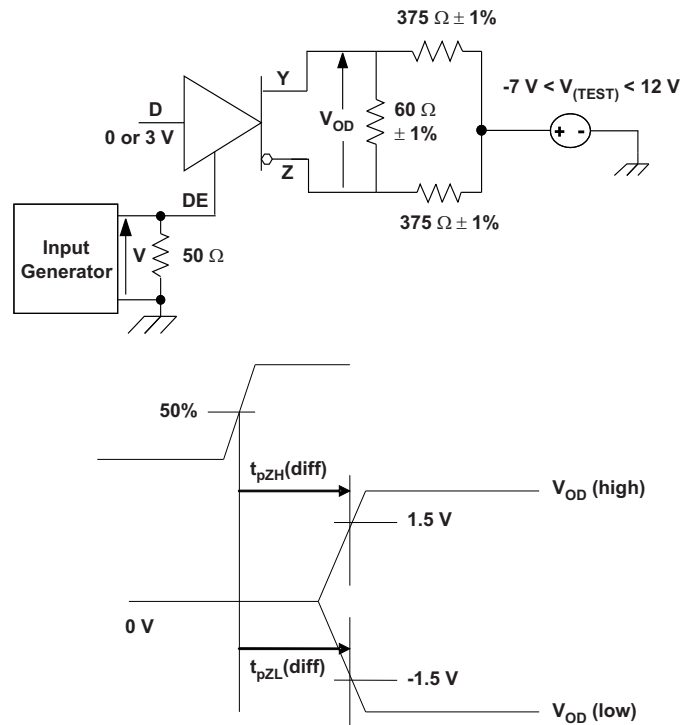


Figure 29. Driver Enable Time From DE to V_{OD}

The time t_{pZL}(x) is the measure from DE to V_{OD}(x). V_{OD} is valid when it is greater than 1.5 V.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65HVD30D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD30DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD30DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD30DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD31D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD31DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD31DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD31DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD32D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD32DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD32DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD32DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD34D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD34DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD34DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD34DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD35D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD35DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD35DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD35DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN65HVD30, SN65HVD33 :

- Enhanced Product: [SN65HVD30-EP](#), [SN65HVD33-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



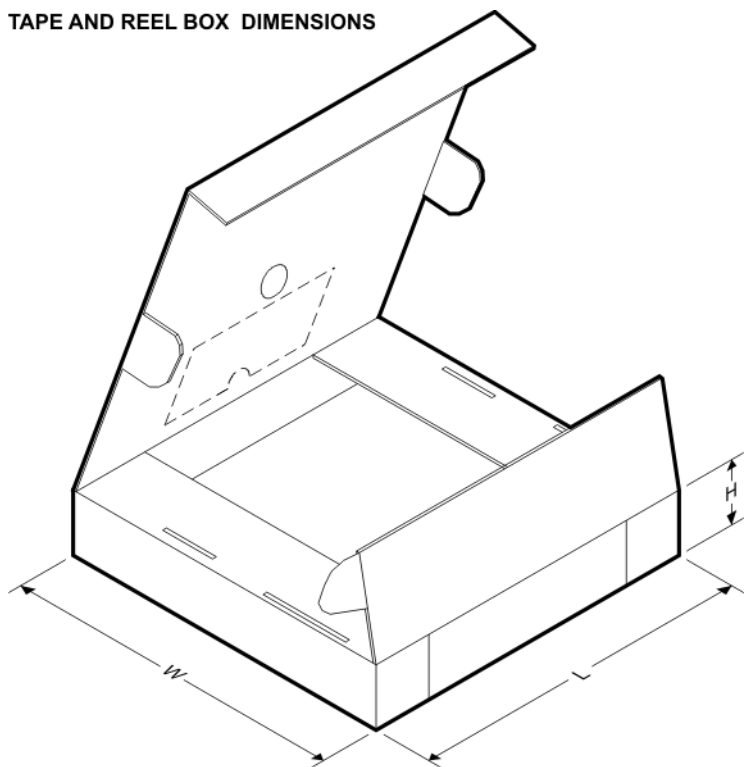
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD31DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD32DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD33DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD34DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD35DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

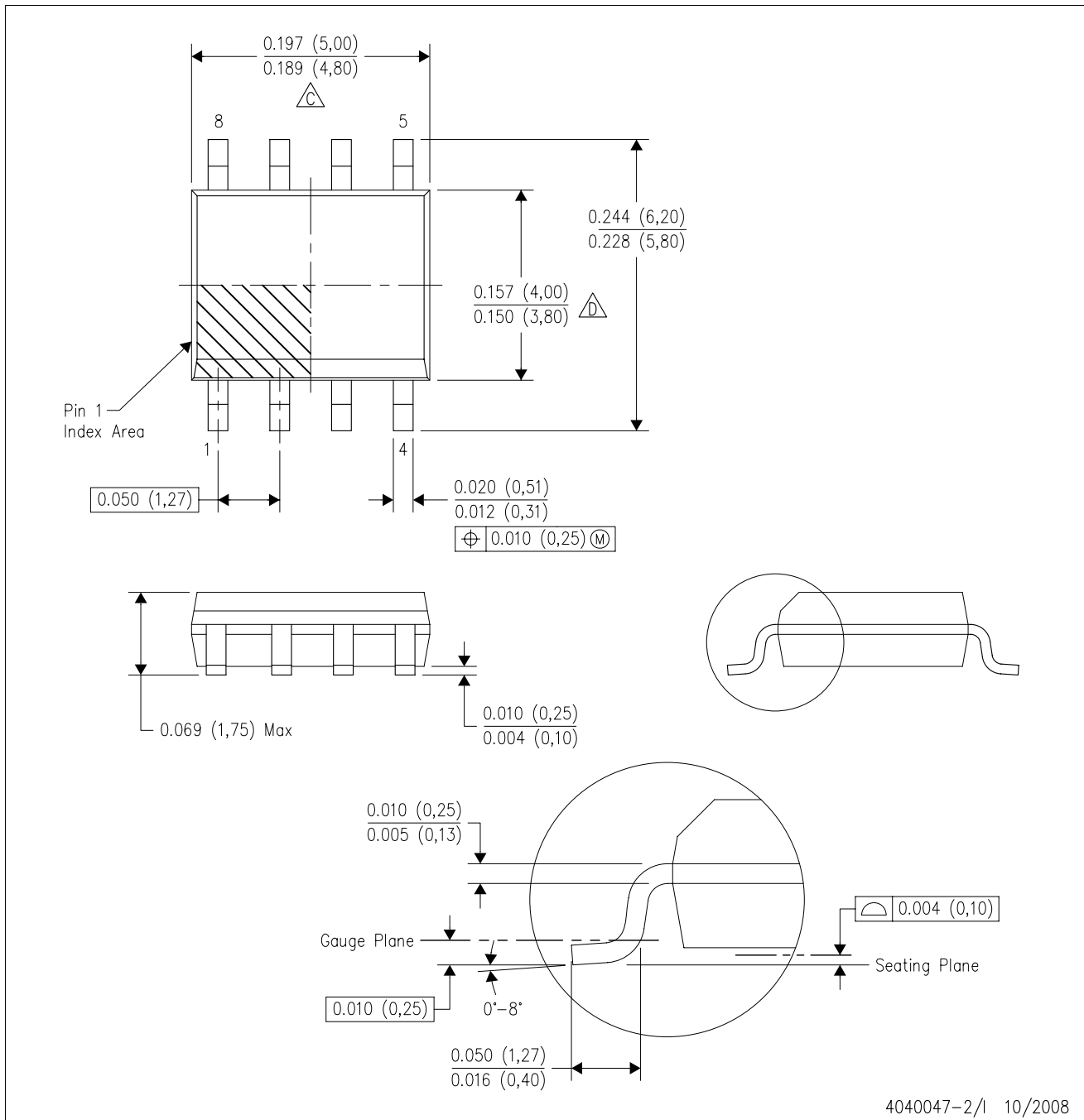


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD30DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD31DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD32DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD33DR	SOIC	D	14	2500	346.0	346.0	33.0
SN65HVD34DR	SOIC	D	14	2500	346.0	346.0	33.0
SN65HVD35DR	SOIC	D	14	2500	346.0	346.0	33.0

D (R-PDSO-G8)

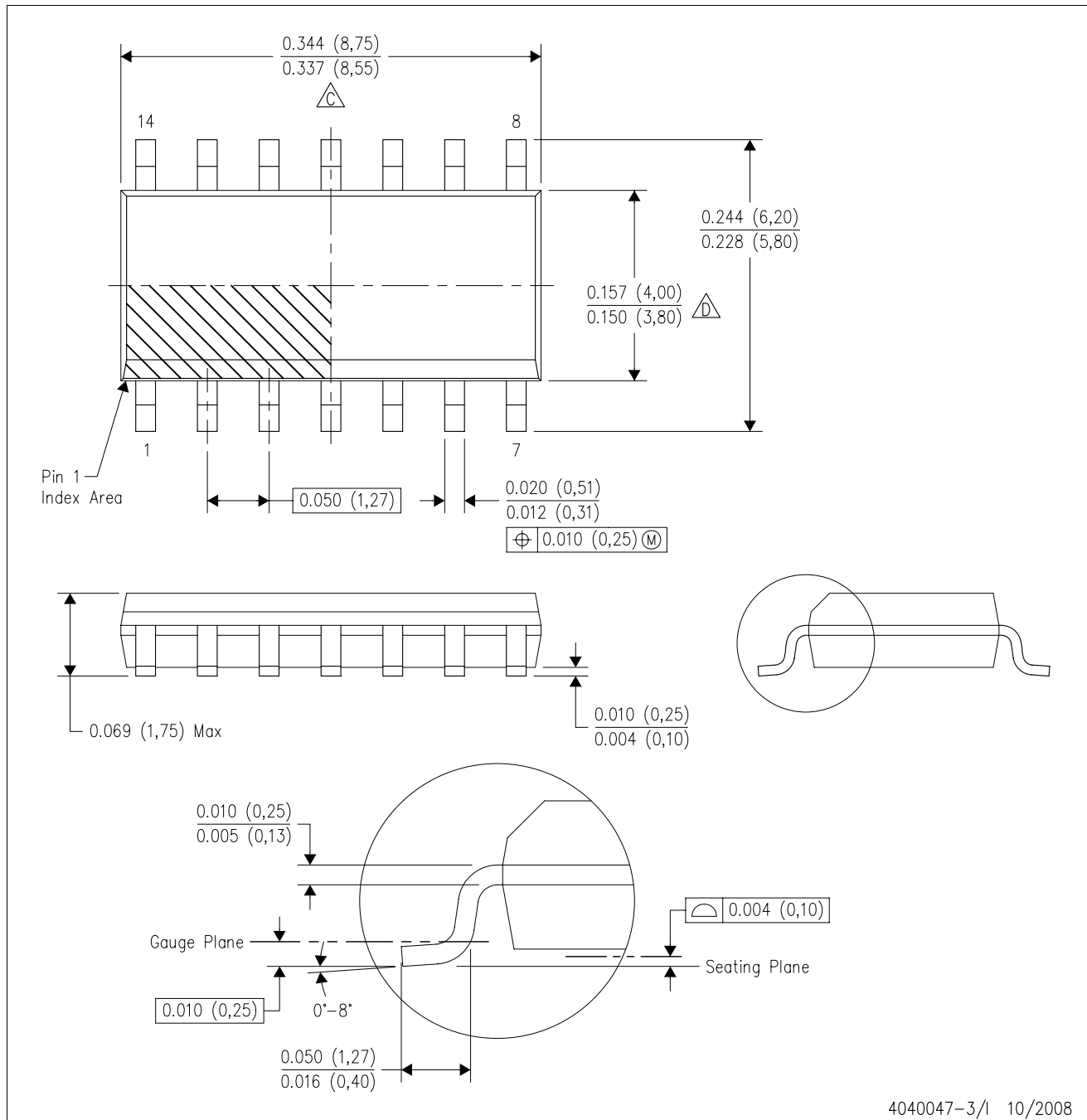
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

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